LAYER STACKUP :

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.80mil	3.5	
3	TOP	Copper	1.60mil		
4	Dielectric 1	RO4835 LOPRO	4.00mil	3.66	
5	L2	Copper	1.20mil		
6	Dielectric2	FR4 370HR	2.85mil	3.9	
7	Dielectric 3	FR4 370HR	2.85mil	3.9	
8	L3	Copper	1.20mil		
9	Dielectric4	FR4 370HR	28.00mil	4.36	
10	L4	Copper	1.20mil		
11	Dielectric5	FR4 370HR	2.92mil	3.9	
12	Dielectric 6	FR4 370HR	2.92mil	3.9	
13	L5	Copper	1.20mil		
14	Dielectric7	FR4 370HR	4.00mil	4.26	
15	BOTTOM	Copper	1.60mil		
16	Bottom Solder	Solder Resist	0.80mil	3.5	
17	Bottom Overlay				

L1-L2 [5]

L1-L6

THIS IS AN IMPEDANCE CONTROLLED BOARD.

NOTE :

EXTERNAL LAYER CU THICKNESSES ARE FINISHED THICKNESS AFTER PLATING.

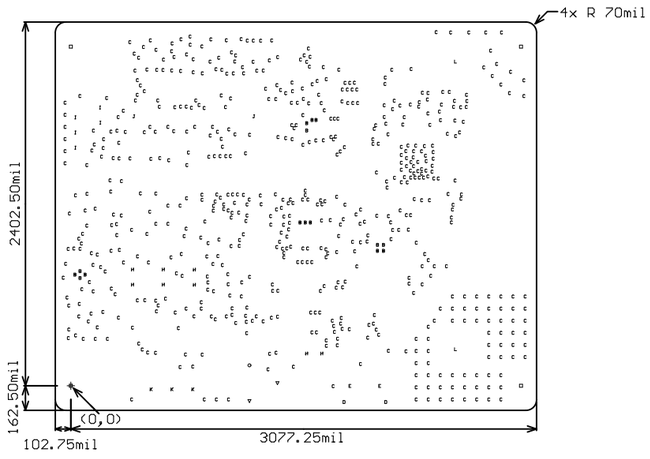
[5] IMPEDANCE TABLE :

LAYER NO	CONDUCTOR WIDTH	DIFF. PAIR SPACING	CPWG SPACING	IMPEDANCE +/-10%	REFERENCE GND
1 (TOP)	7.08mil	N/A	6.73mil	50ohm	GND
1 (TOP)	5.2mil	5mil	N/A	100ohm	GND

DRILL CHART :

Symbol	Count	Hole Size	Plated	Hole Type	Hole Length	Routed Path Length	Drill Layer Pair	Hole Tolerance
B	15	7.87mil (0.200mm)	PTH	Round	-	-	TOP - BOTTOM	+0.00mil/-7.87mil
C	621	12.20mil (0.310mm)	PTH	Round	-	-	TOP - BOTTOM	+0.00mil/-12.20mil
D	2	23.62mil (0.600mm)	PTH	Slot	51.18mil (1.300mm)	27.56mil (0.700mm)	TOP - BOTTOM	+/-3.00mil
E	2	33.47mil (0.850mm)	PTH	Round	-	-	TOP - BOTTOM	+/-3.00mil
∇	2	39.37mil (1.000mm)	PTH	Slot	118.11mil (3.000mm)	78.74mil (2.000mm)	TOP - BOTTOM	+/-3.00mil
O	1	39.37mil (1.000mm)	PTH	Slot	137.80mil (3.500mm)	98.43mil (2.500mm)	TOP - BOTTOM	+/-3.00mil
H	8	40.00mil (1.016mm)	PTH	Round	-	-	TOP - BOTTOM	+/-3.00mil
J	2	40.16mil (1.020mm)	NPTH	Round	-	-	TOP - BOTTOM	+/-2.00mil
I	5	40.16mil (1.020mm)	PTH	Round	-	-	TOP - BOTTOM	+/-3.00mil
K	3	47.24mil (1.200mm)	PTH	Round	-	-	TOP - BOTTOM	+/-3.00mil
L	2	157.48mil (4.000mm)	PTH	Round	-	-	TOP - BOTTOM	+/-3.00mil
□	4	160.00mil (4.064mm)	NPTH	Round	-	-	TOP - BOTTOM	+/-2.00mil
	667 Total							

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



NOTES : UNLESS OTHERWISE SPECIFIED.

1. ALL VIAS ARE TENTED ON BOTH SIDES UNLESS SOLDERMASK OPENED IN GERBER.
2. ALL VIAS ON PAD INCLUDING BGA AREA SHOULD BE FILLED WITH NON CONDUCTIVE EPOXY AND SURFACE SHOULD BE FLAT
   THERE ARE MANY VIAS ON THE PCB WHICH ARE EITHER ON THE PADS OR CLOSE TO PADS
   THESE NEED TO BE FILLED WITH A NON-CONDUCTIVE EPOXY TO ENSURE FLAT SURFACE.
   BGA AREA VIAS SHOULD BE CAPPED WITH COPPER PLATING TO ENSURE FLAT SURFACE
   FLATNESS TOLERANCE FOR VIA ON PADS: +0.000 /- 0.001 INCHES ON BOTH SIDES.
3. MANUFACTURER'S IDENTIFICATION, DATECODE LETTER SHALL BE SILKSCREENED ON SOLDER SIDE OF THE BOARD.
4. TRACE WIDTH SHOULD BE ACCURATELY ETCHED. MAX TOLERANCE +/- 1 MIL
5. [5] FOR IMPEDANCE DETAILS REFER STACKUP & IMPEDANCE TABLE.
6. SOLDER MASK OPENING IS KEPT SAME SIZE AS PAD (1:1) FOR ALL COMPONENTS EXCEPT U2
   THE MANUFACTURER IS REQUESTED TO SIZE IT AS PER THEIR SOLDERMASK TOLERANCE.
   FOR U2 (BGA) PLEASE FOLLOW SAME SOLDERMASK SIZE AS GERBER
7. [7] SURFACE FINISH: IMMERSION SILVER
8. [8] SOLDERMASK ON BOTH SIDES OF THE BOARD SHALL BE LPI, COLOR RED.
9. FOR ANTENNA ETCHING TOLERANCE REFER "ANTENNA ETCHING REQUIREMETS" DOCUMENT.
10. THE FOUR GND NET ANTENNAS NEAR Y1 ARE INTENTIONAL

DESIGN INFORMATION

MIN. TRACK WIDTH: 3.9 MIL
MIN. CLEARANCE: 3.9 MIL
MIN. VIA PAD SIZE: 13.77MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 2 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
☐ FR-408 ☐ FR-4 High Tg ☒ OTHER REFER STACKUP
THICKNESS: ☐ 62 MIL (1.6mm) +/-10% ☒ OTHER 57.14 MIL +/-10%
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/- _____

DRILLING:
REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER _____

BOARD FINISH:
SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER _____
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER REFER NOTE [8]
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☐ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☒ OTHER REFER NOTE [7]

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☐ N.C. ROUTE ☒ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
☐ XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE
☐ XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE
☐ OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE
☐ LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

TEXAS INSTRUMENTS

PROJECT TITLE: PROC010
DESIGNED FOR: Public Release
FILE NAME: PROC010B_PCB.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PROC010	REV: B	SVN REV: Not In VersionControl
LAYER NAME = FAB	TID #: N/A		
	GENERATED : 8/24/2018 10:01:11 AM	TEXAS INSTRUMENTS	

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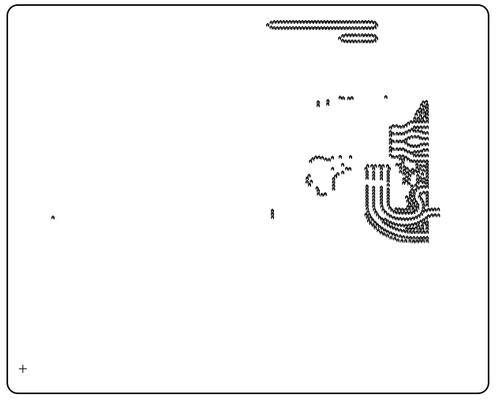
ENGINEER:	LAYOUT BY:
Adrian Ozer	Tessolve
SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1.5.472

WO # : 307314-7312-D

DRILL CHART :

Symbol	Count	Hole Size	Plated	Hole Type	Hole Length	Routed Path Length	Drill Layer Pair	Tolerance
A	508	5.90mil (0.150mm)	PTH	Round	-	-	TOP - L2	+0.00mil/-5.90mil
	508 Total							



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LAYER NAME = FAB	TID #: N/A		
	GENERATED : 8/24/2018 10:01:16 AM		TEXAS INSTRUMENTS

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TEXAS INSTRUMENTS

PROJECT TITLE: PROC010	
DESIGNED FOR: Public Release	
FILE NAME: PROC010B_PCB.PcbDoc	
ENGINEER: Adrian Ozer	LAYOUT BY: Tessolve
SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1.5.472

WO # : 307314-7312-D